Section 17. Electrical Specifications

17.1 Absolute Maximum Ratings

Table 17-1 lists the absolute maximum ratings.

Table 17-1. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.3 to +7.0	V
Programming voltage	V_{PP}	–0.3 to +13.5	V
Input voltage			
Ports 1 – 6, 8, 9	V_{in}	–0.3 to V_{CC} + 0.3	V
Port 7	V_{in}	–0.3 to AV_{CC} + 0.3	V
Analog supply voltage	AV_{CC}	–0.3 to +7.0	V
Analog input voltage	V_{AN}	–0.3 to AV_{CC} + 0.3	V
Operating temperature	T_{opr}	Regular specifications: –20 to +75	°C
		Wide-range specifications: – 40 to +85	°C
Storage temperature	T_{stg}	–55 to +125	°C

Note: The input pins have protection circuits that guard against high static voltages and electric fields, but these high input-impedance circuits should never receive overvoltages exceeding the absolute maximum ratings shown in table 17-1.

17.2 Electrical Characteristics

17.2.1 DC Characteristics

Table 17-2 lists the DC characteristics of the H8/330.

Table 17-2. DC Characteristics

Conditions: V_{CC} = 5.0V ±10%*, AV_{CC} = 5.0V ±10%, V_{SS} = AV_{SS} = 0V,
Ta = –20 to 75°C (regular specifications), Ta = –40 to 85°C (wide-range specifications)

Item		Symbol	min	typ	max	Unit	Measurement conditions
Schmitt trigger input voltage (1)	$P6_7$ – $P6_2$, $P6_0$, $P8_6$ – $P8_0$,	V_T^-	1.0	–	–	V	
		V_T^+	–	–	3.5	V	
	$P9_7$, $P9_4$ – $P9_0$	$V_T^+ - V_T^-$	0.4	–	–	V	
Input High voltage (2)	$\overline{RES}$, $\overline{STBY}$, MD_1, MD_0	V_{IH}	V_{CC} – 0.7	–	V_{CC} + 0.3	V	
	EXTAL, $\overline{NMI}$		V_{CC} × 0.7	–	V_{CC} + 0.3	V	
	$P7_7$ – $P7_0$		2.2	–	AV_{CC} + 0.3	V	
Input High voltage	Input pins other than (1) and (2)	V_{IH}	2.2	–	V_{CC} + 0.3	V	
Input Low voltage (3)	$\overline{RES}$, $\overline{STBY}$ MD_1, MD_0	V_{IL}	–0.3	–	0.5	V	
Input Low voltage	Input pins other than (1) and (3)	V_{IL}	–0.3	–	0.8	V	
Output High voltage	All output pins	V_{OH}	V_{CC} – 0.5	–	–	V	I_{OH} = –200µA
			3.5	–	–	V	I_{OH} = –1.0mA
Output Low voltage	All output pins	V_{OL}	–	–	0.4	V	I_{OL} = 1.6mA
	Ports 1 and 2		–	–	1.0	V	I_{OL} = 10.0mA
Input leakage current	$\overline{RES}$	$\|I_{inl}\|$	–	–	10.0	µA	V_{in} = 0.5V to V_{CC} – 0.5V
	$\overline{STBY}$, $\overline{NMI}$, MD_1, MD_0		–	–	1.0	µA	
	$P7_7$ – $P7_0$		–	–	1.0	µA	V_{in} = 0.5V to AV_{CC} – 0.5V
Leakage current in 3-state (off state)	Ports 1, 2, 3 4, 5, 6, 8, 9	$\|I_{TSI}\|$	–	–	1.0	µA	V_{in} = 0.5V to V_{CC} – 0.5V
Input pull-up MOS current	Ports 1, 2, 3 4, 5, 6, 8, 9	-Ip	30	–	250	µA	V_{in} = 0V

* Connect AV_{CC} to the power supply (+5V) even when the A/D converter is not used.

Table 17-2. DC Characteristics (cont.)

Conditions: V_{CC} = AV_{CC} = 5.0V ±10%, V_{SS} = AV_{SS} = 0V, Ta = –20 to 75°C (regular specifications)
Ta = –40 to 85°C (wide-range specifications)

Item		Symbol	min	typ	max	Unit	Measurement conditions
Input capacitance	$\overline{RES}$ (V_{PP})	C_{in}	–	–	60	pF	V_{in} = 0V
	$\overline{NMI}$		–	–	30	pF	
	All input pins except $\overline{RES}$ and $\overline{NMI}$		–	–	15	pF	f = 1MHz Ta = 25°C
Current dissipation*1	Normal operation	I_{CC}	–	12	25	*m*A	f = 6MHz
			–	16	30	*m*A	f = 8MHz
			–	20	40	*m*A	f = 10MHz
	Sleep mode		–	8	15	*m*A	f = 6MHz
			–	10	20	*m*A	f = 8MHz
			–	12	25	*m*A	f = 10MHz
	Standby modes*2		–	0.01	5.0	µA	
Analog supply current	During A/D conversion	AI_{CC}	–	0.6	1.5	*m*A	
	Waiting		–	0.01	5.0	µA	
RAM standby voltage		V_{RAM}	2.0	–	–	V	

*1 Current dissipation values assume that $V_{IH\ min.}$ = V_{CC} – 0.5V, $V_{IL\ max.}$ = 0.5V, all output pins are in the no-load state, and all MOS input pull-ups are off.

*2 For these values it is assumed that $V_{RAM} \leq V_{CC} < 4.5V$ and $V_{IH\ min.}$ = $V_{CC} \times 0.9$, $V_{IL\ max.}$ = 0.3V.

Table 17-2. DC Characteristics (3V Version) (preliminary)

Conditions: V_{CC} = 3.0V ±10%, AV_{CC} = 5.0V ±10%*1, V_{SS} = AV_{SS} = 0V, Ta = 0 to 70°C

Item		Symbol	min	typ	max	Unit	Measurement conditions
Schmitt trigger input voltage*2 (1)	$P6_7$ – $P6_2$, $P6_0$, $P8_6$ – $P8_0$, $P9_7$, $P9_4$ – $P9_0$	V_{T^-}	V_{CC} × 0.15	–	–	V	
		V_{T^+}	–	–	V_{CC} × 0.7	V	
		V_{T^+}–V_{T^-}	0.2	–	–	V	
Input High voltage*2 (2)	$\overline{RES}$, $\overline{STBY}$ MD_1, MD_0 EXTAL, $\overline{NMI}$	V_{IH}	V_{CC} × 0.9	–	V_{CC} + 0.3	V	
	$P7_7$ – $P7_0$		2.0	–	AV_{CC} + 0.3	V	
	Input pins other than (1) and (2) above		2.0	–	V_{CC} + 0.3	V	
Input Low voltage*2 (3)	$\overline{RES}$, $\overline{STBY}$ MD_1, MD_0	V_{IL}	–0.3	–	V_{CC} × 0.1	V	
	Input pins other than (1) and (3) above		–0.3	–	0.6	V	
Output High voltage	All output pins	V_{OH}	2.4	–	–	V	I_{OH} = –500μA
			V_{CC} – 0.2	–	–	V	I_{OH} = –20μA
Output Low voltage	All output pins	V_{OL}	–	–	0.4	V	I_{OL} = 1.2mA
	Ports 1 and 2		–	–	0.4	V	I_{OL} = 2.0mA
Input leakage current	$\overline{RES}$	|I_{in}|	–	–	10.0	μA	V_{in} = 0.5 to
	$\overline{STBY}$, $\overline{NMI}$, MD_1, MD_0		–	–	1.0	μA	V_{CC} – 0.5V
	$P7_7$ – $P7_0$		–	–	1.0	μA	V_{in} = 0.5 to AV_{CC} – 0.5V
Leakage current in 3-state (off state)	Ports 1, 2, 3 4, 5, 6, 8, 9	|I_{TSI}|	–	–	1.0	μA	V_{in} = 0.5 to V_{CC} – 0.5V
Input pull-up MOS current	Ports 1, 2, 3	$-I_p$	3	–	120	μA	V_{in} = 5.0V

Notes: *1 Connect AV_{CC} to the power supply (+3V) even when the A/D converter is not used.

*2 In the range 3.3V < V_{CC} < 4.5V, for the input levels of V_{IH} and V_{T^+}, apply the higher of the values given for the 5V and 3V versions. For V_{IL} and V_{T^-}, apply the lower of the values given for the 5V and 3V versions.

Table 17-2. DC Characteristics (3V Version) (preliminary) (cont.)

Conditions: V_{CC} = 3.0V ±10%, AV_{CC} = 5.0V ±10%*1, V_{SS} = AV_{SS} = 0V,
Ta = 0 to 70°C

Item		Symbol	min	typ	max	Unit	Measurement conditions
Input capacitance	$\overline{RES}$	C_{in}	–	–	60	pF	V_{in} = 0V
	$\overline{NMI}$		–	–	30	pF	f = 1MHz
	All input pins except $\overline{RES}$ and $\overline{NMI}$		–	–	15	pF	Ta = 25°C
Current dissipation*1	Normal operation	I_{CC}	–	6	–	mA	f = 3MHz
			–	10	15	mA	f = 5MHz, V_{CC} = 3.3 V
	Sleep mode		–	4	–	mA	f = 3MHz
			–	6	10	mA	f = 5MHz, V_{CC} = 3.3 V
	Standby modes*2		–	0.01	5.0	μA	
Analog supply current	during A/D or D/A conversion	AI_{CC}	–	–	1.5	mA	
	Waiting		–	0.01	5.0	μA	
RAM backup voltage (in standby modes)		V_{RAM}	2.0	–	–	V	

Notes: *1 Current dissipation values assume that $V_{IH\ min}$ = V_{CC} – 0.5V, $V_{IL\ max}$ = 0.5V, all output pins are in the no-load state, and all input pull-up transistors are off.

*2 For these values it is assumed that $V_{RAM} \leq V_{CC} < 2.7V$ and $V_{IH\ min}$ = V_{CC} × 0.9, $V_{IL\ max}$ = 0.3V.

Table 17-3. Allowable Output Current Sink Values

Conditions: V_{CC} = AV_{CC} = 5.0V ±10%, V_{SS} = AV_{SS} = 0V,
Ta = –20 to 75°C (regular specifications)
Ta = –40 to 85°C (wide-range specifications)

Item		Symbol	min	typ	max	Unit
Allowable output Low current sink (per pin)	Ports 1 and 2	I_{OL}	–	–	10	mA
	Other output pins		–	–	2.0	mA
Allowable output Low current sink (total)	Ports 1 and 2, total	ΣI_{OL}	–	–	80	mA
	All output pins		–	–	120	mA
Allowable output High current sink (per pin)	All output pins	$-I_{OH}$	–	–	2.0	mA
Allowable output High current sink (total)	Total of all output	$\Sigma - I_{OH}$	–	–	40	mA

Table 17-3. Allowable Output Current Sink Values (3V Version) (Preliminary)

Conditions: Vcc = 3.0V ± 10%, AVcc = 5.0V ± 10%, Vss = AVss = 0V, Ta = −0 to 75°C

Item		Symbol	min	typ	max	Unit
Allowable output Low current sink (per pin)	Ports 1 and 2	I_{OL}	–	–	10	mA
	Other output pins		–	–	2.0	mA
Allowable output Low current sink (total)	Ports 1 and 2, total	ΣI_{OL}	–	–	80	mA
	Total of all output		–	–	120	mA
Allowable output High current sink (per pin)	All output pins	$-I_{OH}$	–	–	2	mA
Allowable output High current sink (total)	Total of all output	$\Sigma - I_{OH}$	–	–	40	mA

Note: To avoid degrading the reliability of the chip, be careful not to exceed the output current sink values in table 17-3. In particular, when driving a Darlington transistor pair or LED directly, be sure to insert a current-limiting resistor in the output path. See figures 17-1 and 17-2.

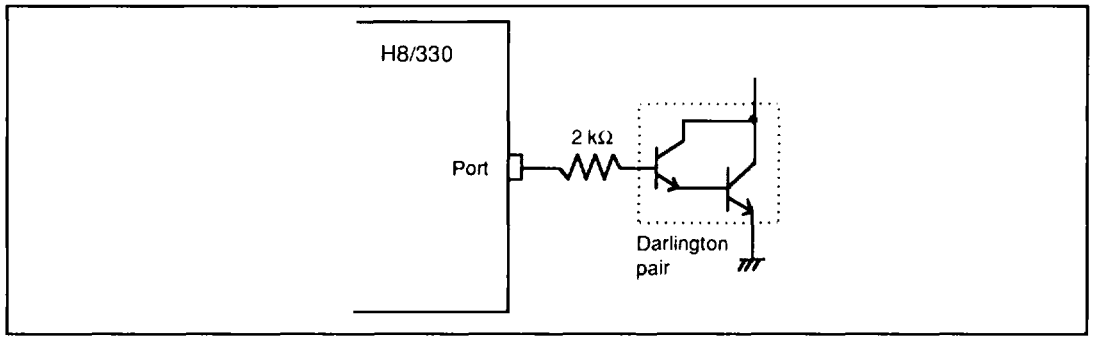


Figure 17-1. Example of Circuit for Driving a Darlington Pair

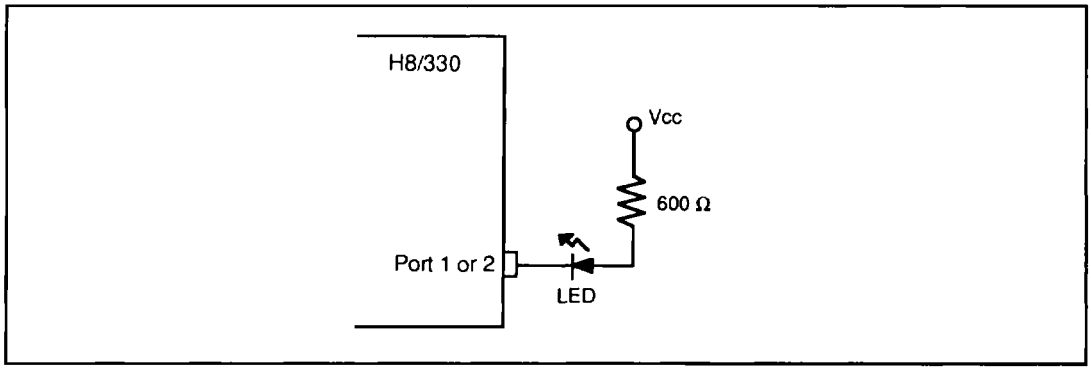


Figure 17-2. Example of Circuit for Driving a LED

17.2.2 AC Characteristics

The AC characteristics of the H8/330 chip are listed in three tables. Bus timing parameters are given in table 17-4, control signal timing parameters in table 17-5, and timing parameters of the on-chip supporting modules in table 17-6.

Table 17-4. Bus Timing

Condition A: V_{CC} = 5.0V ±10%, Ø = 0.5 to 10MHz, V_{SS} = 0V,
Ta = −20 to 75°C (regular specifications),
Ta = −40 to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0V ±10%, V_{SS} = 0V, Ø = 0.5MHz to maximum operating frequency,
Ta = 0 to 75°C

			Condition B		Condition A						
Measurement		Measurement	5MHz		6MHz		8MHz		10MHz		
Item	Symbol	conditions	min	max	min	max	min	max	min	max	Unit
Clock cycle time	t_{cyc}	Fig. 17-4	200	2000	166.7	2000	125	2000	100	2000	ns
Clock pulse width Low	t_{CL}	Fig. 17-4	70	–	65	–	45	–	35	–	ns
Clock pulse width High	t_{CH}	Fig. 17-4	70	–	65	–	45	–	35	–	ns
Clock rise time	t_{Cr}	Fig. 17-4	–	30	–	15	–	15	–	15	ns
Clock fall time	t_{Cf}	Fig. 17-4	–	30	–	15	–	15	–	15	ns
Address delay time	t_{AD}	Fig. 17-4	–	100	–	70	–	60	–	55	ns
Address hold time	t_{AH}	Fig. 17-4	30	–	30	–	25	–	20	–	ns
Address strobe delay time	t_{ASD}	Fig. 17-4	–	90	–	70	–	60	–	50	ns
Write strobe delay time	t_{WSD}	Fig. 17-4	–	120	–	70	–	60	–	50	ns
Strobe delay time	t_{SD}	Fig. 17-4	–	90	–	70	–	60	–	50	ns
Write strobe pulse width	t_{WSW}	Fig. 17-4	200	–	200	–	150	–	120	–	ns
Address setup time 1	t_{AS1}	Fig. 17-4	25	–	25	–	20	–	15	–	ns
Address setup time 2	t_{AS2}	Fig. 17-4	105	–	105	–	80	–	65	–	ns
Read data setup time	t_{RDS}	Fig. 17-4	80	–	70	–	55	–	50	–	ns
Read data hold time	t_{RDH}	Fig. 17-4	10	–	0	–	0	–	0	–	ns
Write data delay time	t_{WDD}	Fig. 17-4	–	140	–	70	–	60	–	60	ns
Read data access time	t_{ACC}	Fig. 17-4	–	300	–	270	–	190	–	160	ns
Write data setup time	t_{WDS}	Fig. 17-4	10	–	30	–	15	–	10	–	ns
Write data hold time	t_{WDH}	Fig. 17-4	30	–	30	–	25	–	20	–	ns
Wait setup time	t_{WTS}	Fig. 17-5	70	–	40	–	40	–	40	–	ns
Wait hold time	t_{WTH}	Fig. 17-5	30	–	10	–	10	–	10	–	ns
E clock delay time	t_{ED}	Fig. 17-6	–	20	–	20	–	20	–	20	ns
E clock rise time	t_{Er}	Fig. 17-6	–	15	–	15	–	15	–	15	ns
E clock fall time	t_{Ef}	Fig. 17-6	–	15	–	15	–	15	–	15	ns
Read data hold time (for E clock)	t_{RDHE}	Fig. 17-6	0	–	0	–	0	–	0	–	ns
Write data hold time (for E clock)	t_{WDHE}	Fig. 17-6	60	–	50	–	40	–	30	–	ns

Table 17-5. Control Signal Timing

Condition A: V_{CC} = 5.0V ±10%, Ø = 0.5 to 10MHz, V_{SS} = 0V,
Ta = −20 to 75°C (regular specifications),
Ta = −40 to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0V ±10%, V_{SS} = 0V, Ø = 0.5MHz to maximum operating frequency,
Ta = 0 to 75°C

Measurement Item	Symbol	Measurement conditions	Condition B 5MHz min	Condition B 5MHz max	Condition A 6MHz min	Condition A 6MHz max	Condition A 8MHz min	Condition A 8MHz max	Condition A 10MHz min	Condition A 10MHz max	Unit
$\overline{RES}$ setup time	t_{RESS}	Fig. 17-7	300	—	200	—	200	—	200	—	ns
$\overline{RES}$ pulse width	t_{RESW}	Fig. 17-7	10	—	10	—	10	—	10	—	tcyc
Mode programming setup time	t_{MDS}	Fig. 17-7	—	—	4	—	4	—	4	—	tcyc
$\overline{NMI}$ setup time ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_7}$)	t_{NMIS}	Fig. 17-8	300	—	110	—	110	—	110	—	ns
$\overline{NMI}$ hold time ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_7}$)	t_{NMIH}	Fig. 17-8	10	—	10	—	10	—	10	—	ns
Interrupt pulse width for recovery from software standby mode ($\overline{NMI}$, $\overline{IRQ_0}$ to $\overline{IRQ_2}$)	t_{NMIW}	Fig. 17-8	300	—	200	—	200	—	200	—	ns
Crystal oscillator settling time (reset)	t_{OSC1}	Fig. 17-9	20	—	20	—	20	—	20	—	ms
Crystal oscillator settling time (software standby)	t_{OSC2}	Fig. 17-10	10	—	10	—	10	—	10	—	ms

Table 17-6. Timing Conditions of On-Chip Supporting Modules

Condition A: V_{CC} = 5.0V ±10%, Ø = 0.5 to 10MHz, V_{SS} = 0V,
Ta = −20 to 75°C (regular specifications),
Ta = −40 to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0V ±10%, V_{SS} = 0V, Ø = 0.5MHz to maximum operating frequency,
Ta = −20 to 75°C

	Item	Symbol	Measurement conditions	Condition B 5MHz min	Condition B 5MHz max	Condition A 6MHz min	Condition A 6MHz max	Condition A 8MHz min	Condition A 8MHz max	Condition A 10MHz min	Condition A 10MHz max	Unit
FRT	Timer output delay time	t_{FTOD}	Fig. 17-11	—	200	—	100	—	100	—	100	ns
	Timer input setup time	t_{FTIS}	Fig. 17-11	100	—	50	—	50	—	50	—	ns
	Timer clock input setup time	t_{FTCS}	Fig. 17-12	100	—	50	—	50	—	50	—	ns
	Timer clock pulse width	t_{FTCWH}	Fig. 17-12	1.5	—	1.5	—	1.5	—	1.5	—	tcyc

Table 17-6. Timing Conditions of On-Chip Supporting Modules (cont.)

Condition A: V_{CC} = 5.0V ±10%, Ø = 0.5 to 10MHz, V_{SS} = 0V,
Ta = −20 to 75°C (regular specifications),
Ta = −40 to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0V ±10%, V_{SS} = 0V, Ø = 0.5MHz to maximum operating frequency,
Ta = 0 to 75°C

				Condition B		Condition A						
			Measurement	5MHz		6MHz		8MHz		10MHz		
	Item	Symbol	conditions	min	max	min	max	min	max	min	max	Unit
TMR	Timer output delay time	t_{TMOD}	Fig. 17-13	—	200	—	100	—	100	—	100	ns
	Timer reset input setup time	t_{TMRS}	Fig. 17-15	100	—	50	—	50	—	50	—	ns
	Timer clock input setup time	t_{TMCS}	Fig. 17-14	100	—	50	—	50	—	50	—	ns
	Timer clock pulse width (single edge)	t_{TMCWH}	Fig. 17-14	1.5	—	1.5	—	1.5	—	1.5	—	t_{cyc}
	Timer clock pulse width (both edges)	t_{TMCWL}	Fig. 17-14	2.5	—	2.5	—	2.5	—	2.5	—	t_{cyc}
PWM	Timer output delay time	t_{PWOD}	Fig. 17-16	—	200	—	100	—	100	—	100	ns
SCI	Input clock (Async)	t_{Scyc}	Fig. 17-17	2	—	2	—	2	—	2	—	t_{cyc}
	(Sync) cycle	t_{Scyc}	Fig. 17-17	4	—	4	—	4	—	4	—	t_{cyc}
	Transmit data delay time (Sync)	t_{TXD}	Fig. 17-17	—	200	—	100	—	100	—	100	ns
	Receive data setup time (Sync)	t_{RXS}	Fig. 17-17	100	—	100	—	100	—	100	—	ns
	Receive data hold time (Sync)	t_{RXH}	Fig. 17-17	100	—	100	—	100	—	100	—	ns
	Input clock pulse width	t_{SCKW}	Fig. 17-18	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{Scyc}
Ports	Output data delay time	t_{PWD}	Fig. 17-19	—	200	—	100	—	100	—	100	ns
	Input data setup time	t_{PRS}	Fig. 17-19	200	—	50	—	50	—	50	—	ns
	Input data hold time	t_{PRH}	Fig. 17-19	200	—	50	—	50	—	50	—	ns

Table 17-6. Timing Conditions of On-Chip Supporting Modules (cont.)

Condition A: V_{CC} = 5.0V ±10%, Ø = 0.5 to 10MHz, V_{SS} = 0V,
Ta = −20 to 75°C (regular specifications),
Ta = −40 to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0V ±10%, V_{SS} = 0V, Ø = 0.5MHz to maximum operating frequency,
Ta = 0 to 75°C

				Condition B		Condition A						
			Measurement	5MHz		6MHz		8MHz		10MHz		
	Item	Symbol	conditions	min	max	min	max	min	max	min	max	Unit
Dual-port RAM read cycle	Address access time	t_{DAA}	Fig. 17-20	–	150	–	150	–	150	–	150	ns
	$\overline{CS}$ access time	t_{DACS}	Fig. 17-20	–	130	–	130	–	130	–	130	ns
	$\overline{OE}$ output delay time	t_{DOE}	Fig. 17-20	–	70	–	70	–	70	–	70	ns
	$\overline{CS}$ output floating time	t_{DCHZ}	Fig. 17-20	–	50	–	50	–	50	–	50	ns
	$\overline{OE}$ output floating time	t_{DOHZ}	Fig. 17-20	–	50	–	50	–	50	–	50	ns
	Output data hold time	t_{DOH}	Fig. 17-20	0	–	0	–	0	–	0	–	ns
Dual-port RAM write cycle	Chip select time	t_{DCW}	Fig. 17-21	100	–	100	–	100	–	100	–	ns
	Address valid time	t_{DAW}	Fig. 17-21	100	–	100	–	100	–	100	–	ns
	Address setup time	t_{DAS}	Fig. 17-21	20	–	20	–	20	–	20	–	ns
	Write pulse width	t_{DWP}	Fig. 17-21	90	–	90	–	90	–	90	–	ns
	Address hold time	t_{DWR}	Fig. 17-21	20	–	20	–	20	–	20	–	ns
	Input data setup time	t_{DDW}	Fig. 17-21	60	–	60	–	60	–	60	–	ns
	Input data hold time	t_{DDH}	Fig. 17-21	15	–	15	–	15	–	15	–	ns

• **Measurement Conditions for AC Characteristics**

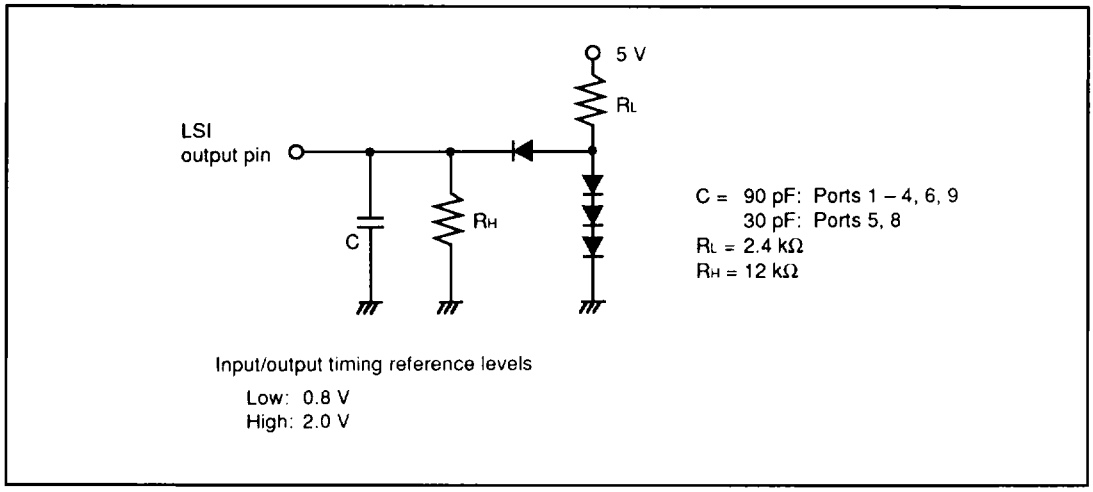


Figure 17-3. Output Load Circuit

17.2.3 A/D Converter Characteristics

Table 17-7 lists the characteristics of the on-chip A/D converter.

Table 17-7. A/D Converter Characteristics

Condition A: V_{CC} = AV_{CC} = 5.0V ±10%, V_{SS} = AV_{SS} = 0V,
Ta = −20 to 75°C (regular specifications),
Ta = −40 to 85°C (wide-range specifications)

Condition B: V_{CC} = 3.0V ±10%, AV_{CC} = 5.0V ±10%, V_{SS} = AV_{SS} = 0V, Ø = 0.5MHz to maximum operating frequency, Ta = 0 to 75°C

	Condition B			Condition A									
	5MHz			6MHz			8MHz			10MHz			
Item	min	typ	max	min	typ	max	min	typ	max	min	typ	max	Unit
Resolution	8	8	8	8	8	8	8	8	8	8	8	8	Bits
Conversion time (single mode)	–	–	24.4	–	–	20.4	–	–	15.25	–	–	12.2	µs
Analog input capacitance	–	–	20	–	–	20	–	–	20	–	–	20	pF
Allowable signal source impedance	–	–	10	–	–	10	–	–	10	–	–	10	kΩ
Nonlinearity error	–	–	±1	–	–	±1	–	–	±1	–	–	±1	LSB
Offset error	–	–	±1	–	–	±1	–	–	±1	–	–	±1	LSB
Full-scale error	–	–	±1	–	–	±1	–	–	±1	–	–	±1	LSB
Quantizing error	–	–	±0.5	–	–	±0.5	–	–	±0.5	–	–	±0.5	LSB
Absolute accuracy	–	–	±1.5	–	–	±1.5	–	–	±1.5	–	–	±1.5	LSB

17.3 MCU Operational Timing

This section provides the following timing charts:

17.3.1 Bus Timing

(1) Basic Bus Cycle (Without Wait States) in Expanded Modes

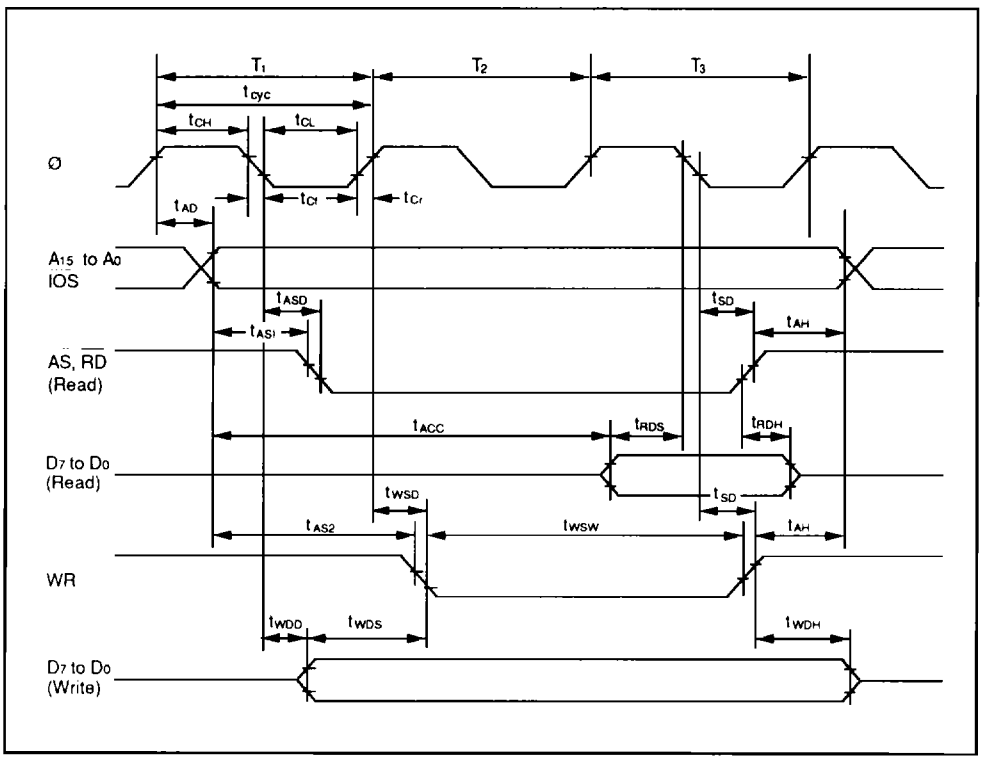


Figure 17-4. Basic Bus Cycle (Without Wait States) in Expanded Modes

(2) Basic Bus Cycle (With 1 Wait State) in Expanded Modes

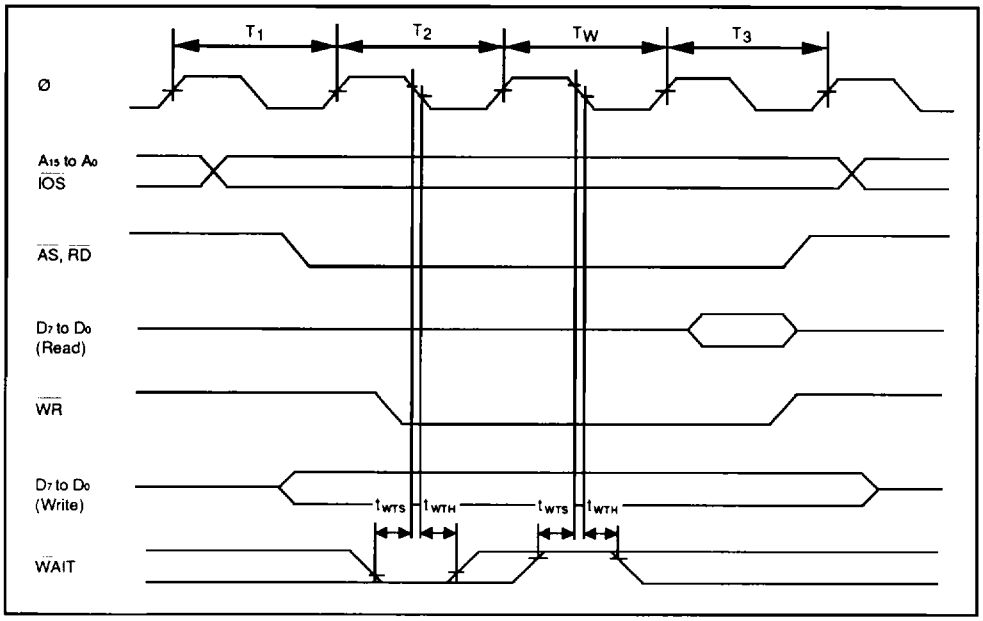


Figure 17-5. Basic Bus Cycle (With 1 Wait State) in Expanded Modes

(3) E Clock Bus Cycle

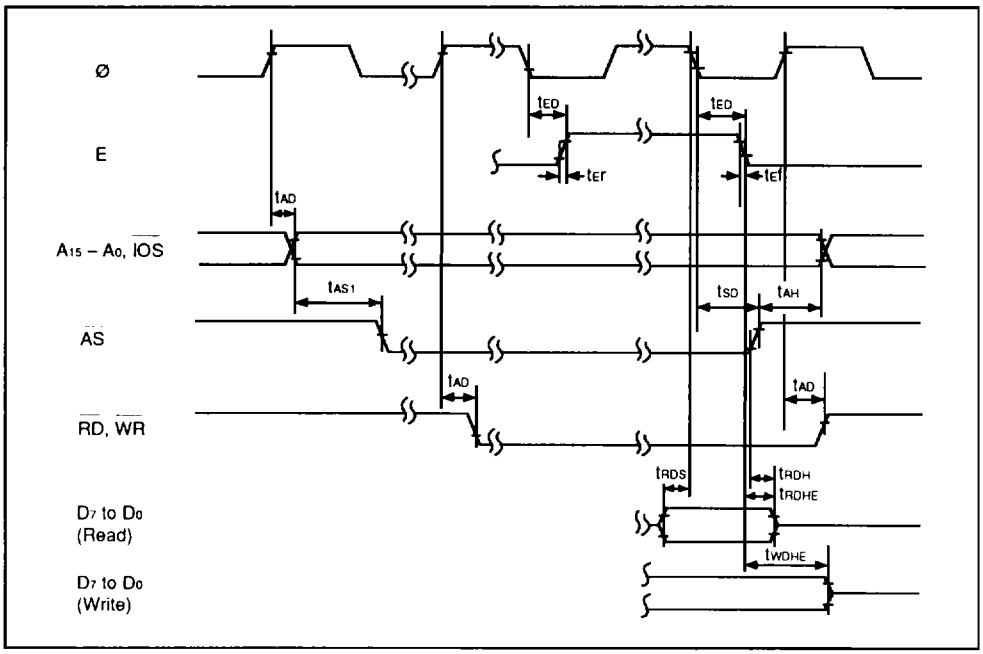


Figure 17-6. E Clock Bus Cycle

17.3.2 Control Signal Timing

(1) Reset Input Timing

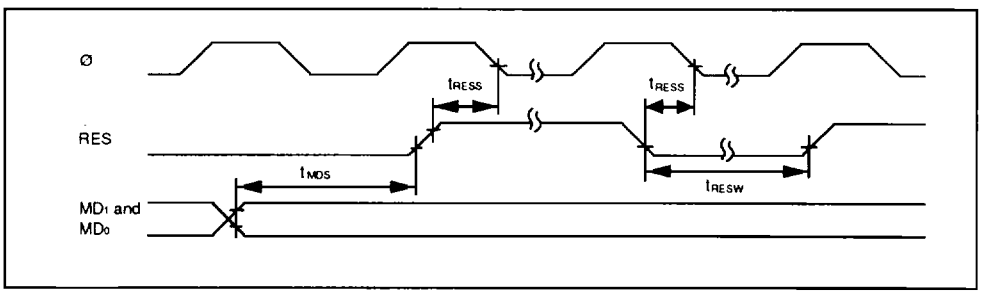


Figure 17-7. Reset Input Timing

(2) Interrupt Input Timing

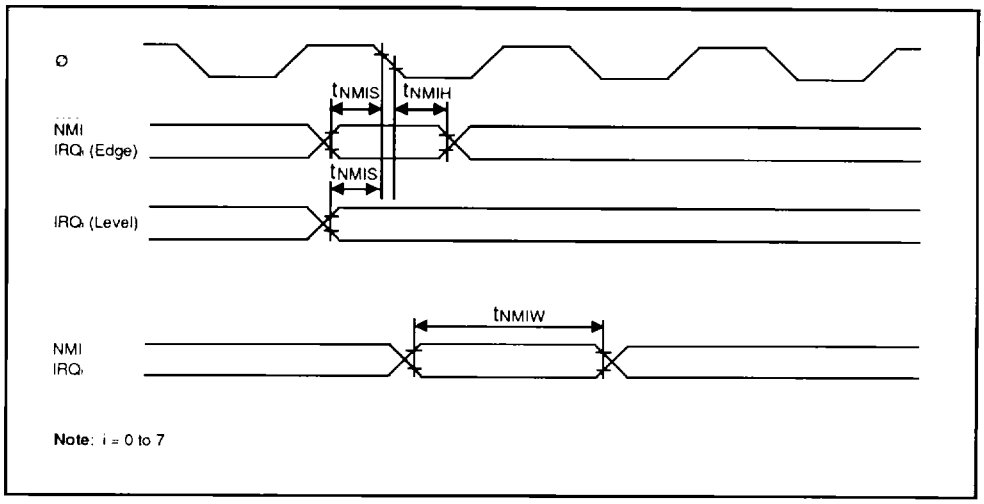


Figure 17-8. Interrupt Input Timing

(3) Clock Settling Timing

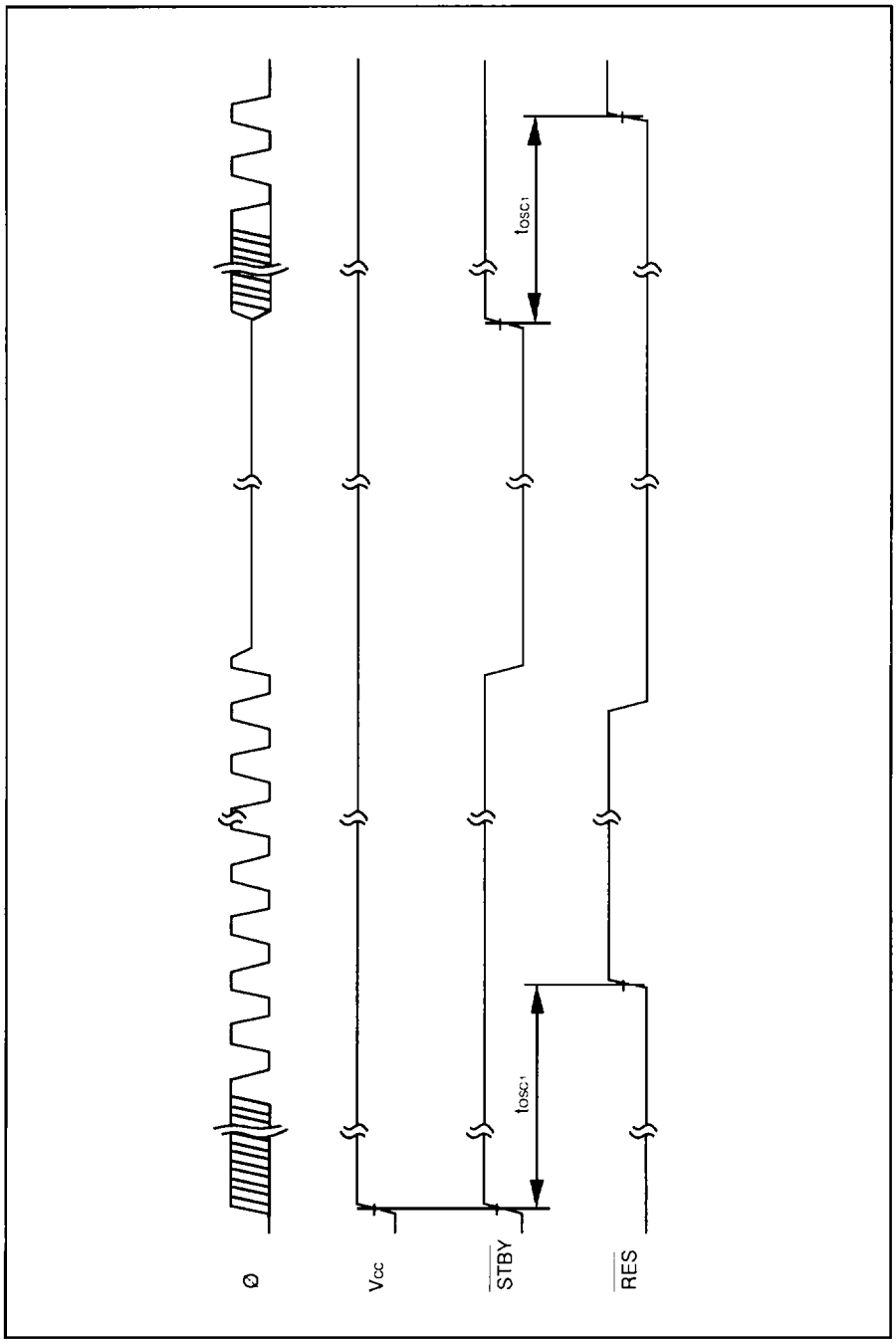


Figure 17-9. Clock Settling Timing

(4) Clock Settling Timing for Recovery from Software Standby Mode

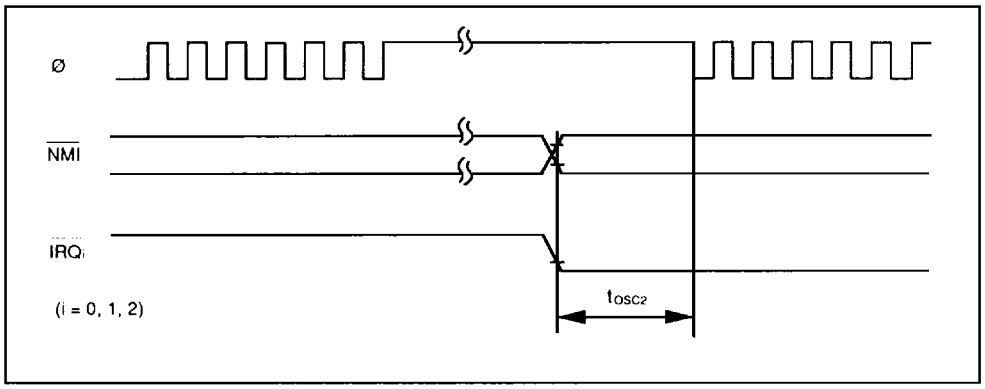


Figure 17-10. Clock Settling Timing for Recovery from Software Standby Mode

17.3.3 16-Bit Free-Running Timer Timing

(1) Free-Running Timer Input/Output Timing

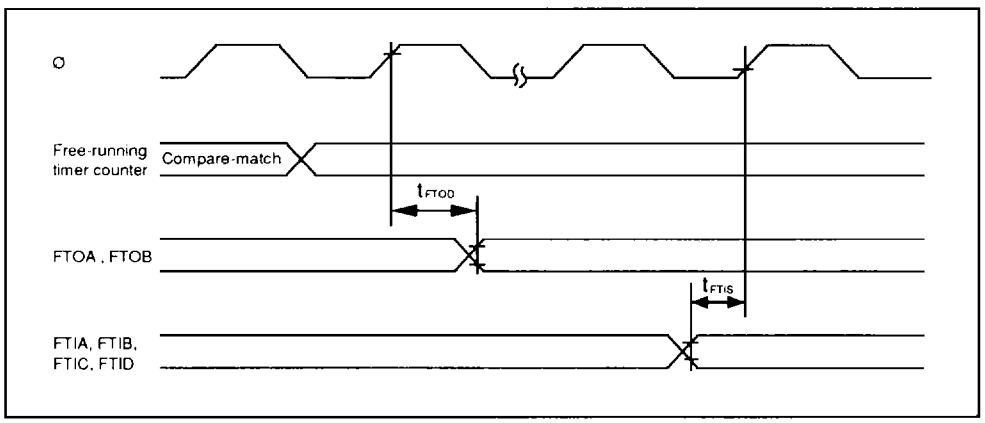


Figure 17-11. Free-Running Timer Input/Output Timing

(2) External Clock Input Timing for Free-Running Timer

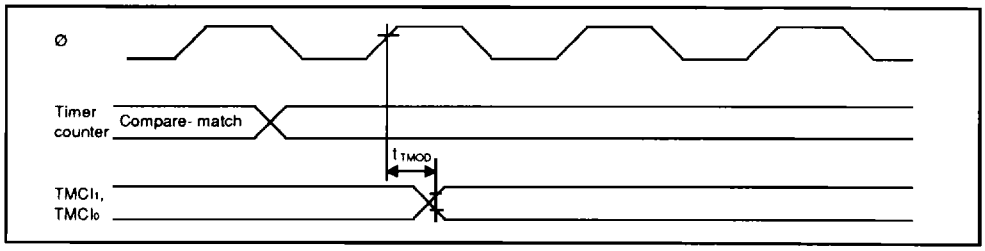


Figure 17-12. External Clock Input Timing for Free-Running Timer

17.3.4 8-Bit Timer Timing

(1) 8-Bit Timer Output Timing

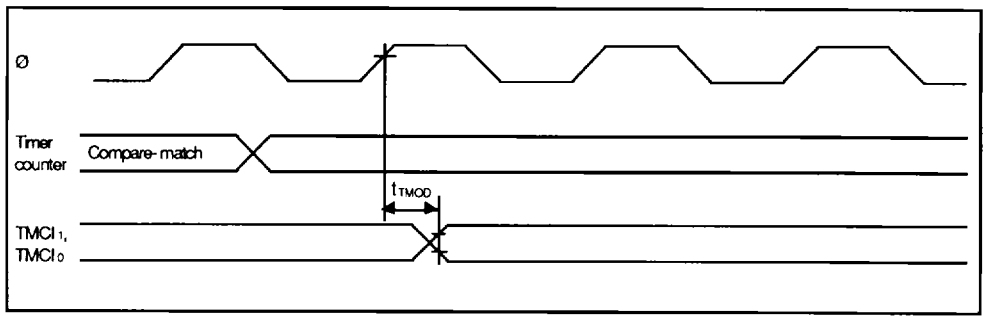


Figure 17-13. 8-Bit Timer Output Timing

(2) 8-Bit Timer Clock Input Timing

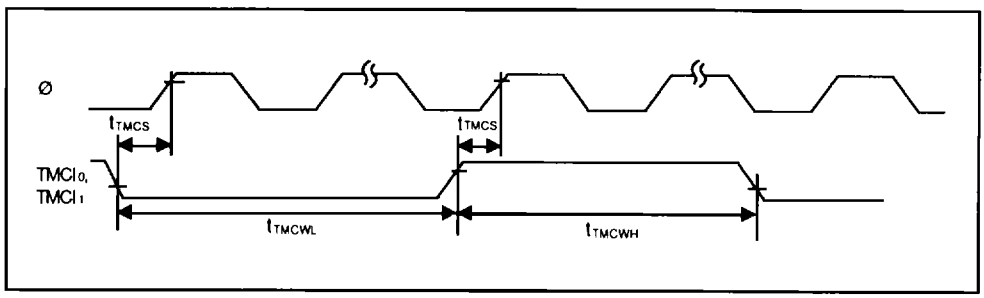


Figure 17-14. 8-Bit Timer Clock Input Timing

(3) 8-Bit Timer Reset Input Timing

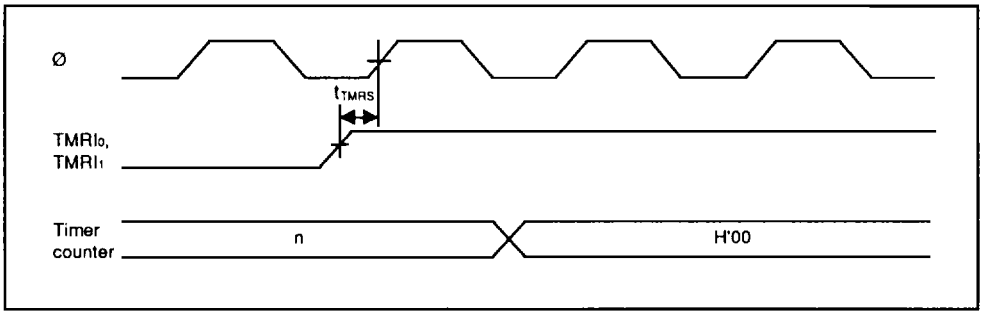


Figure 17-15. 8-Bit Timer Reset Input Timing

17.3.5 Pulse Width Modulation Timer Timing

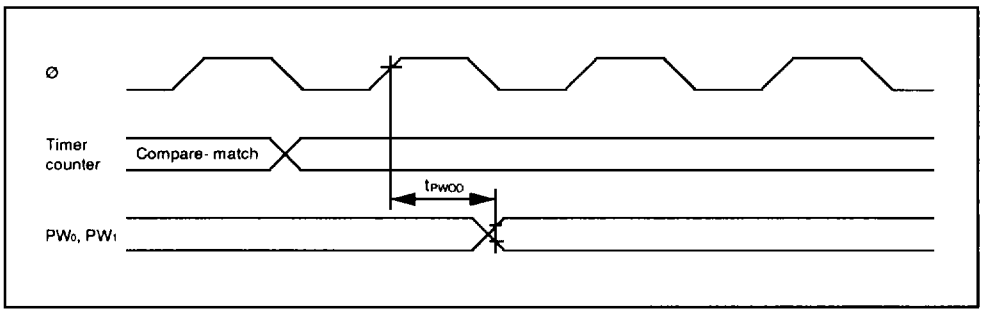


Figure 17-16. PWM Timer Output Timing

17.3.6 Serial Communication Interface Timing

(1) SCI Input/Output Timing

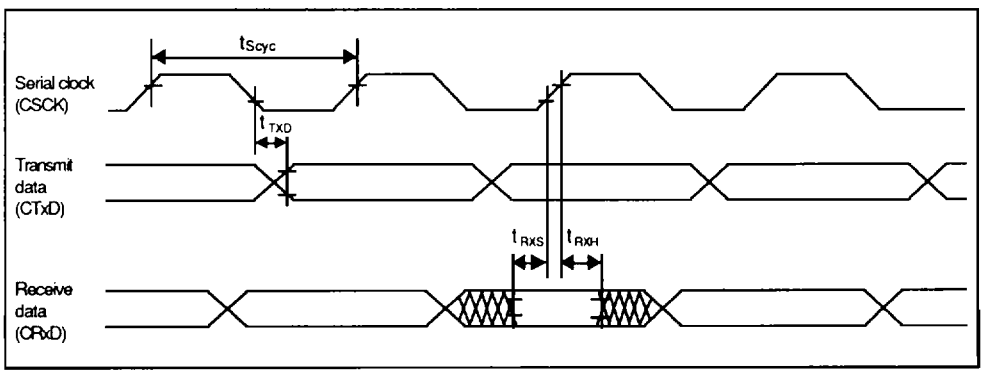


Figure 17-17. SCI Input/Output Timing (Synchronous Mode)

(2) SCI Input Clock Timing

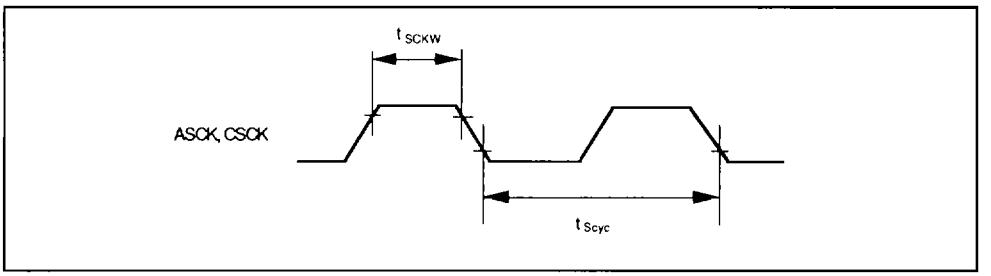


Figure 17-18. SCI Input Clock Timing

17.3.7 I/O Port Timing

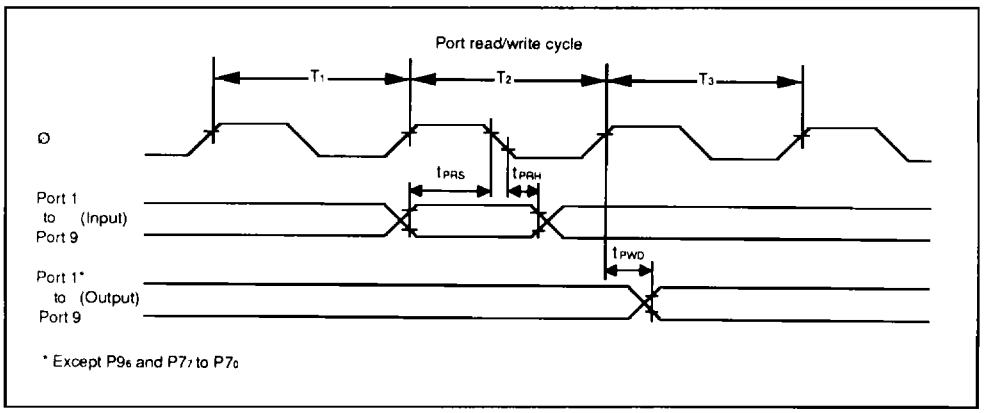
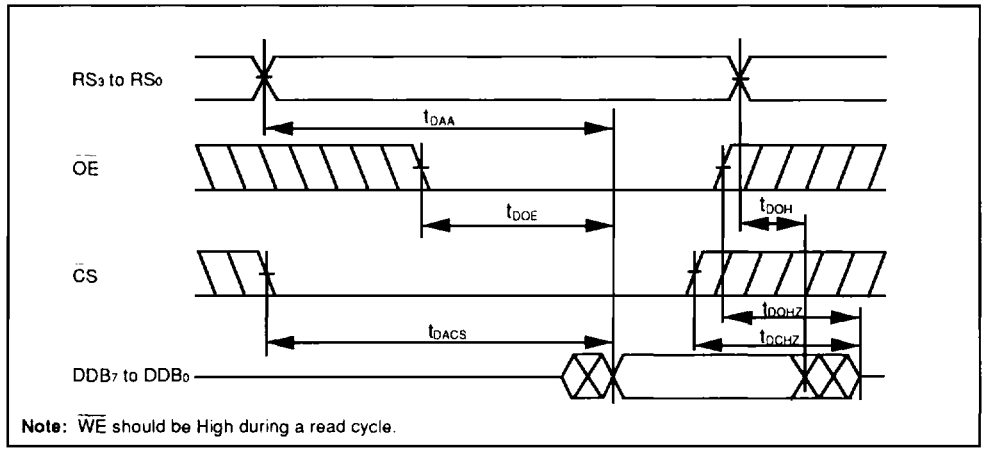


Figure 17-19. I/O Port Input/Output Timing

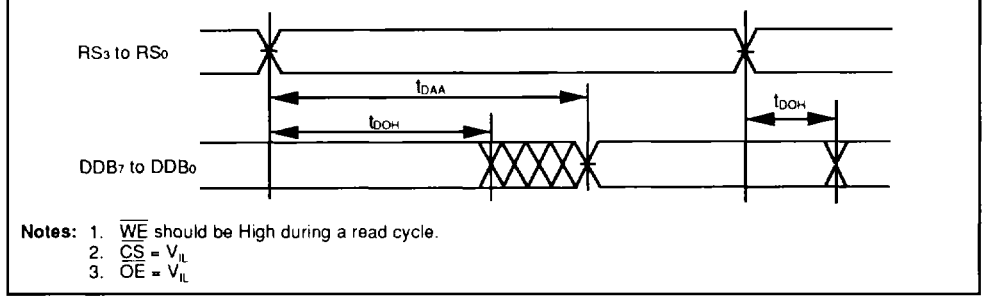
17.3.8 Dual-Port RAM Timing

(1) Read Cycle 1



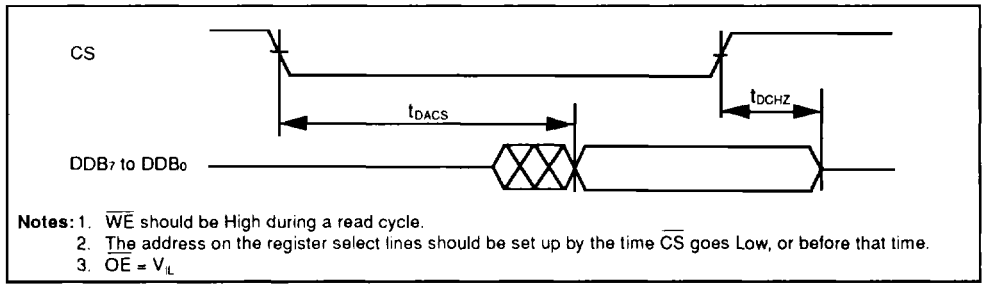
Note: $\overline{WE}$ should be High during a read cycle.

(2) Read Cycle 2



Notes: 1. $\overline{WE}$ should be High during a read cycle.
2. $\overline{CS} = V_{IL}$
3. $\overline{OE} = V_{IL}$

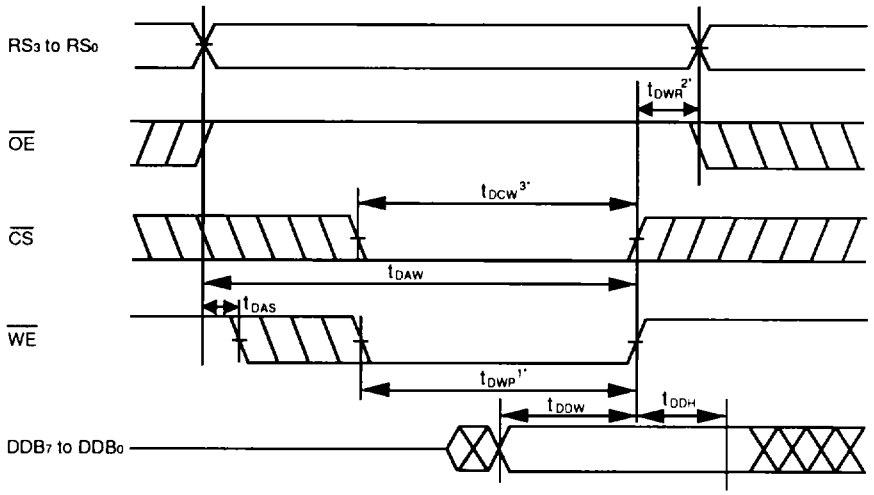
(3) Read Cycle 3



Notes: 1. $\overline{WE}$ should be High during a read cycle.
2. The address on the register select lines should be set up by the time $\overline{CS}$ goes Low, or before that time.
3. $\overline{OE} = V_{IL}$

Figure 17-20. Dual-Port RAM Read Timing

(4) Write Cycle



Notes: 1. Data are written while $\overline{CS}$ and $\overline{WE}$ are both low (t_{DWP}).
2. t_{DWR} is measured from the rise of $\overline{CS}$ or $\overline{WE}$, whichever rises first.
3. If $\overline{CS}$ goes Low at the same time as $\overline{WE}$ goes Low or after $\overline{WE}$ goes Low, the output remains in the high-impedance state.

Figure 17-21. Dual-Port RAM Write Timing